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The Large Hadron Collider Project *IT-XXXX/LHC/LHC*

Technical Specification of LHC instrumentation VME crates Back plane, power supplies and transition modules

Abstract

This Technical Specification concerns the supply of 210 VME crates
Deliveries are foreseen over 4 years from placement of the Contract.

May 2001

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1. INTRODUCTION

This document concerns the VME crate specification for the specific power supplies, the custom back plane and the transition modules required by the CERN AB/BDI group for the implementation of the LHC machine instrumentation. The elements concerned are compatible with the specification developed for the LHC experiments, which are based on VME64x [1]. The specific power supplies, the custom back plane and the mechanical support for the transition modules will be provided within the tender framework developed by the CERN EP Division [2].

2. SCOPE OF THE SPECIFICATION

The objective is to provide a single VME crate structure to be used by all AB/BDI instrumentation experts. The specific features of the VME crates are described in this document. An instrumentation VME crate will contain the following parts:

a) The card cage: The 6 (six) Unit high rack-mounted sub-rack variant 2 with 21 slots and referred to in [2] as "6U Sub-rack Variant 2"
b) The custom-designed back plane
c) The custom-designed power supply
d) The mechanical support for the transition modules (not included variant 2)
e) The fan tray: This two-unit-high modular, removable module beneath the subrack card cage is described in the EP document, however its remote controls will be developed by the CERN AB/CO group. There will not be any further reference to the fan tray in this document

3. USERS REQUIREMENT DESCRIPTION

3.1 The power supply requirements

3.1.1 Mechanical characteristics

The air-cooled power supply module shall be installed at the upper three-unit high part of the back of the VME crate leaving room underneath for transition modules. The power supply module shall be easily installed or removed. The mechanical characteristics of the power supply module shall comply with the EP document [2] while the electrical characteristics are described in this document.

3.1.2 Standard VME voltages and specific voltages

Two specific power supply modules are required. Each power supply module shall contain the standard VME64x power supply voltages and a set of specific voltages.

3.1.3 Standard VME64x power supplies requirements

The standard VME64x voltage and current requirements are listed in table 1 below:

VME64x voltages	Maximum current	Maximum power
3.3 V	50 A	165 W
5.0 V	50 A	250 W
12 V	0.2 A	2.4 W
-12 V	0.2 A	2.4 W

Table 1: Standard VME64x voltages and currents

NB : 48 Volt power supplies are not required.

3.1.4 Specific power supply requirements

3.1.4.1 Reasons for specific voltage and current requirements

The delicate analogue electronics for the beam instrumentation requires specific voltages. The two sets of compatible power supply modules referred to as type A and type B hereafter are specified in tables 2 and 3 respectively:

Type A voltages	Maximum current	Maximum power
+5.0 V	18 A	90 W
-5.2 V	36 A	187 W
-2.0 V	27 A	54 W

Table 2: Specific voltages and currents for type A

Type B voltages	Maximum current	Maximum power
+5.0 V	18 A	90 W
+15 V	4.8 A	72 W
-15 V	4.8 A	72 W

Table 3: Specific voltages and currents for type B

NB: The “specific”+5 Volt supply is distinct from the standard VME64x +5 Volt supply.

3.1.4.2 Referencing specific voltages

The specific voltages shall be distributed via a bus on the back plane in floating mode. The appropriate connection to *the zero-volt analogue reference* will be established by the instrumentation experts within the VME boards as outlined in figures 1 and 2 below:

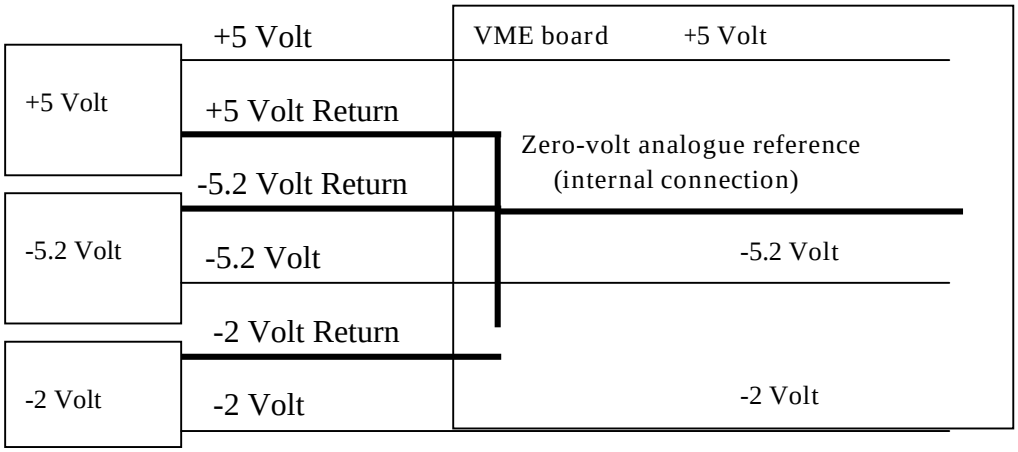

Figure 1: Referencing specific voltages for the type A power supply

NB: The term “Return” refers to the mains of the power supply closest to the cage voltage.

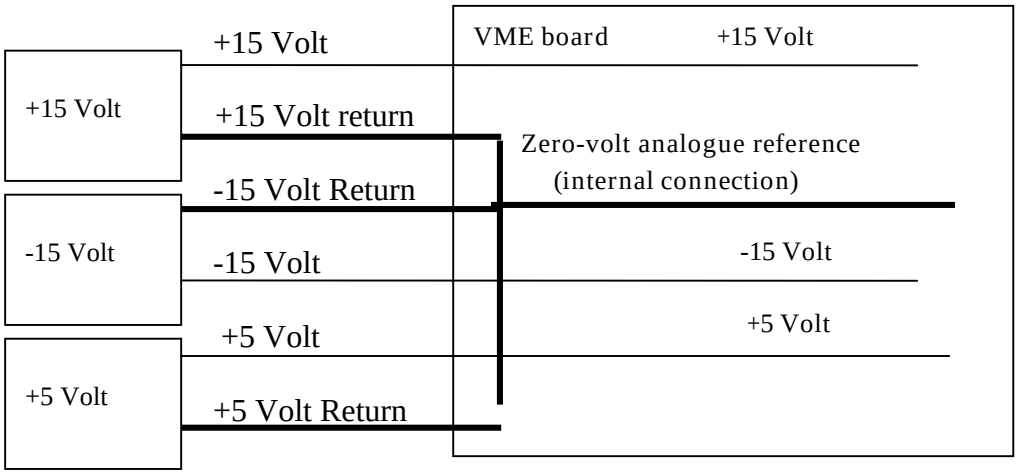

Figure 2: Referencing specific voltages for the type B power supply

3.1.4.3 Electrical characteristics of the specific voltages

The electrical characteristics of power supplies are specified in EP document with the exception of the parameters listed in table 4 below for the voltages indicated in 3-1-4-1 :

Parameters and conditions	Limits
Maximum output change for a +/- 10% input voltage (230 V) variation	<0.1%
Maximum output change for a 100% load variation	<0.1%
Temperature coefficient	< 0.02% par ºC
Residual noise measured on a 20 MHz oscilloscope	< 20mV

Table 4: Specific power supply requirements

3.1.5 Electrical protection

The back plane shall be equipped with an identification means, which shall be read by the internal controller of the modular power supply at insertion time. All the voltages shall be delivered onto the back plane, hence to the VME boards, only after the back plane has been identified and accepted.
All other protection features are described in the EP document [2].

3.1.6 Grounding connection

An easily accessible and clearly visible means to connect and disconnect the mains earth to and from the DC 0V shall be provided. No special tools shall be required to change the ground connection as specified in the EP document [2].

NB: The grounding of the *Zero-volt analogue reference* is not considered and will be left floating.

3.2 The custom-designed back plane features

The back plane shall be monolithic. There is only one type of custom back plane. It shall have the J1 and the J2/RJ2 connectors as specified in the VME64x document [1] on all 21 positions. The J1 and the J2/RJ2 connectors will both have 5 rows of pins.
The specific characteristics of this custom back plane concern only the 19x5 pin J0 connector installed on slot 3 included to slot 21 included, slot 1 and slot 2 are not equipped with the J0 connector.

3.3 Specific connections on J0

3.3.1 Generals

The specific connections on the custom-designed back plane concern only the J0 connector.

3.3.2 Various types of connections are listed below

a) Distribution of specific type A and type B power supplies

b) Distribution of two sets of timing signals (see figure 3 below)
c) Distribution of general purpose bus lines
d) Distribution of general purpose power lines
f) Connection via Daisy chain

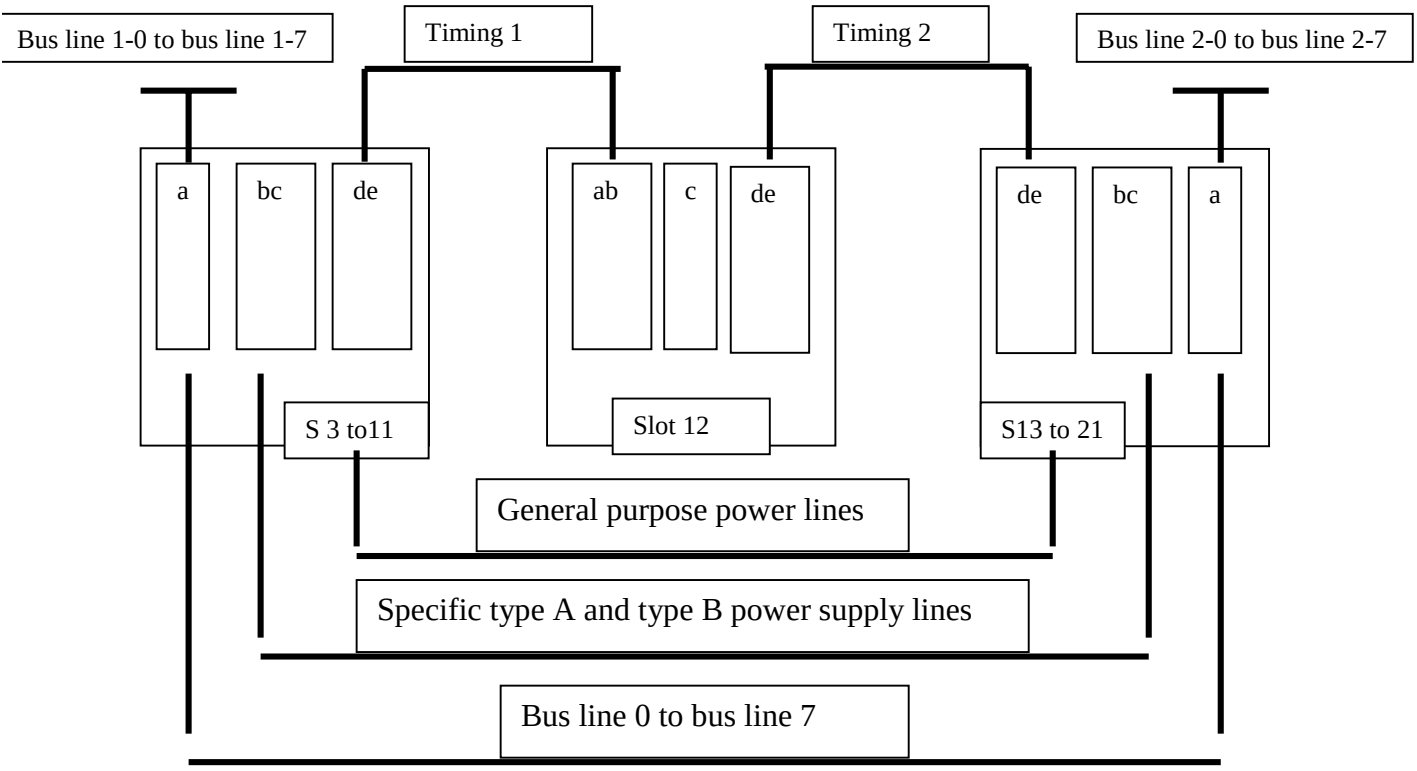

Figure 3: The layout of the connections on J0

3.3.2.1 Power supply to back plane connection

The two power supplies shall be interchangeable and compatible with the unique custom-designed back plane.

All the five voltages provided by both types A and type B power supplies (+15 Volt, +5 Volt, -2 Volt, -5.2 Volt and –15 Volt) shall be distributed via the J0 connector

i) from slot 3 included to slot 11 included and
ii) from slot 13 included to slot 21 included,
iii) slot 12 will use only standard VME64x voltages.

Table 5 below indicates the maximum current ratings per VME board. Table 6a and table 6b show the pin allocations for the J0 connector for modules installed in slots 3 to 11 or in slots 13 to 21 respectively.

Type	Voltage	Maximum current
A and B	+5.0 V	1.0 A
A	-5.2 V	2.0 A
A	-2.0 V	1.5 A
B	+15 V	0.4 A
B	-15 V	0.4 A

Table 5: Maximum current ratings per VME board

NB: Remote monitoring of power supplies will conform to EP document [2].

Voltage drop: The maximum voltage difference on a power line will be less than 0.3%, excluding the voltage drop in the connector. The measurement is made between two slots separated by a single non-powered slot.

3.3.2.2 Distribution of timing signals

There are two sets of timing signals distributed on the J0 connector. These timing signals will be generated by the VME board in slot 12. One set of timing signals concerns slot 3 (included) to slot 11(included), the second set concerns slot 13 (included) to slot 21(included). The distribution consists in parallel lines from the VME board in slot 12
The pins allocation for the timing signals are shown in table 6a for the slots 3 to 11 and in table 6b for slots 13 to 21 respectively. The pin allocation for the VME board in slot 12 is shown in table 7.
The LVDS timing signals must be terminated in slot 3 and in slot 21 for the two sets of timing signals respectively. The routing of the fast LVDS signals must comply with IEEE1596.3; for more information please consult [3], chapter 6.1.1 Multidrop (single termination): http://www.national.com/appinfo/lvds/files/LOM_2.pdf

3.3.2.3 Distribution of bus lines

Two different distributions of bus lines are required. These bus lines will be used to transfer TTL type signals. These two distributions are:

a) Two separated sets of 8 bit-wide bus lines from slot 3 (included) to slot 11 (included) and from slot 13 (included) to slot 21(included) respectively. Slot 12 is not concerned. The pin allocation is shown in table 6a for slots 3 to 11 (see bus lines labelled “1-0” to “1-7”) and in table 6b for slots 13 to 21 (see bus lines labelled “2-0” to “2-7”) respectively.
b) One set of 8 bit-wide bus lines from slot 3 (included) to slot 11(included) and from slot 13 (included) to slot 21(included). Slot 12 is not concerned.
The pin allocation is shown in table 6a and in table 6b (see bus lines labelled “0” to “7”).

3.3.2.4 Distribution of general purpose power lines

One set of seven general purpose power lines is required from slot 3 (included) to slot 11 (included) and from slot 13 (included) to slot 21 (included). Slot 12 is not concerned. The pin allocation is shown in table 6a and in table 6b (see GPPL-0 to GPPL-6).
These lines may be used to transfer power from one VME board to the others. The voltage shall not exceed 48 volt, the maximum current rating shall be 1 Ampere.

3.3.2.5 Connection via Daisy chain

Two separated sets of two daisy chained signal lines will permit to transfer information between two adjacent VME boards. Daisy chain1 shall connect slot 3 (included) to slot 11 (included) and daisy chain2 shall connect slot 13 (included) to 21 (included) respectively. Slot 12 is not concerned.
The configuration is outlined in figure 4 (only one daisy chain shown). These Daisy chain lines may also be used to transfer differential signals, the routing must comply with IEEE1596.3; for more information please consult [3], chapter 6.1.1 Multidrop (single termination): http://www.national.com/appinfo/lvds/files/LOM_2.pdf
It will be the responsibility of the instrument expert to ensure the continuity of the daisy chains at the level of the VME board in the slots.

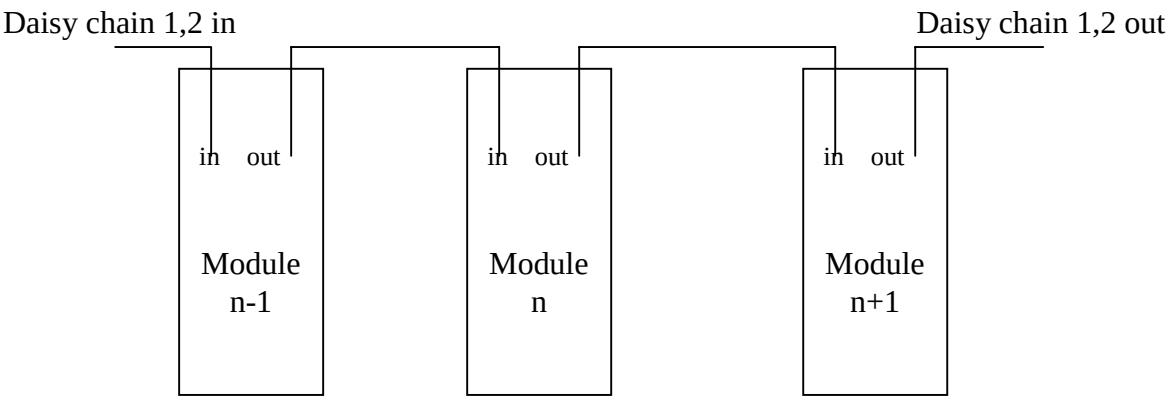

Figure 4: Daisy chain configuration

The four pins reserved for this purpose are shown in table 6a for daisy chain1 and in table 6b for daisy chain2.

3.3.3 Live insertion and extraction

Requested as defined in IT-2916/EP document [2].

3.4 Transition modules

Provision shall be made to allow instrument experts to insert transition modules on all 21 slots on the RJ2 connector whenever necessary whenever they need this facility. The VME crates shall be ready to be equipped on the field with the necessary mechanics to install the transition modules.
The transition modules shall be 3 (three) U high and 160 mm deep.
The RP2 connector mating the RJ2 connector shall have 5 rows of pins.
There will not be any cooling facility for the transition modules.
NB: Reminder: Only +5 V and GND are available on RJ2 connector.

References:

[1] **“**American National Standard for VME64 Extensions”, ANSI/VITA 1.1.1997.

[2] “Technical Specification for Subracks for LHC Experiments”, IT-2916/EP.
[3] http://www.national.com/appinfo/lvds/files/LOM_2.pd

Pos	Row z	Row a	Row b	Row c	Row d	Row e	Row f
1	GND	Bus line-0	-5V2RET	-5V2RET	HW Low Byte 1 bit 0	HW High Byte 1 bit 0	GND
2	GND	Bus line-1	-5V2RET	-5V2RET	HW Low Byte 1 bit 1	HW High Byte 1 bit 1	GND
3	GND	Bus line-2	-5V2RET	-5V2RET	HW Low Byte 1 bit 2	HW High Byte 1 bit 2	GND
4	GND	Bus line-3	-5V2	-5V2	HW Low Byte 1 bit 3	HW High Byte 1 bit 3	GND
5	GND	Bus line-4	-5V2	-5V2	HW Low Byte 1 bit 4	HW High Byte 1 bit 4	GND
6	GND	Bus line-5	-5V2	-5V2	HW Low Byte 1 bit 5	HW High Byte 1 bit 5	GND
7	GND	Bus line-6	-2VRET	-2VRET	HW Low Byte 1 bit 6	HW High Byte 1 bit 6	GND
8	GND	Bus line-7	-2VRET	-2VRET	HW Low Byte 1 bit 7	HW High Byte 1 bit 7	GND
9	GND	GPPL-0	-2V	-2V	Daisy chain1- 1-in	Daisy chain1-1-out	GND
10	GND	GPPL-1	-2V	-2V	Daisy chain 1-2-in	Daisy chain 1-2-out	GND
11	GND	GPPL-2	GPPL-3	GPPL-4	GPPL-5	GPPL-6	GND
12	GND	Bus line1-0	+5V	+5V	Bunch Select 1 Bit 0	LVDS Turn clock Delay 1 +	GND
13	GND	Bus line1-1	+5V	+5V	Bunch Select 1 Bit 1	LVDS Turn clock Delay 1 -	GND
14	GND	Bus line1-2	+5VRET	+5VRET	Bunch Select 1 Bit 2	TTL Turn clock Delay 1 +	GND
15	GND	Bus line1-3	+5VRET	+5VRET	Bunch Select 1 Bit 3	TTL Turn clock Delay 1 -	GND
16	GND	Bus line1-4	+15V	+15V	Bunch Select 1 Bit 4	LVDS 40 MHz Clock 1 +	GND
17	GND	Bus line1-5	+15VRET	+15VRET	Bunch Select 1 Bit 5	LVDS 40 MHz Clock 1 -	GND
18	GND	Bus line1-6	-15VRET	-15VRET	Bunch Select 1 Bit 6	TTL 40 MHz Clock 1 +	GND
19	GND	Bus line1-7	-15V	-15V	Bunch Select 1 Bit 7	TTL 40 MHz Clock 1 -	GND

Table 6a: Pin allocations on J0 for slots 3 to 11 (Front view)

Pos	Row z	Row a	Row b	Row c	Row d	Row e	Row f
1	GND	Bus line-0	-5V2RET	-5V2RET	HW Low Byte 2 bit 0	HW High Byte 2 bit 0	GND
2	GND	Bus line-1	-5V2RET	-5V2RET	HW Low Byte 2 bit 1	HW High Byte 2 bit 1	GND
3	GND	Bus line-2	-5V2RET	-5V2RET	HW Low Byte 2 bit 2	HW High Byte 2 bit 2	GND
4	GND	Bus line-3	-5V2	-5V2	HW Low Byte 2 bit 3	HW High Byte 2 bit 3	GND
5	GND	Bus line-4	-5V2	-5V2	HW Low Byte 2 bit 4	HW High Byte 2 bit 4	GND
6	GND	Bus line-5	-5V2	-5V2	HW Low Byte 2 bit 5	HW High Byte 2 bit 5	GND
7	GND	Bus line-6	-2VRET	-2VRET	HW Low Byte 2 bit 6	HW High Byte 2 bit 6	GND
8	GND	Bus line-7	-2VRET	-2VRET	HW Low Byte 2 bit 7	HW High Byte 2 bit 7	GND
9	GND	GPPL-0	-2V	-2V	Daisy chain 2- 1-in	Daisy chain 2-1-out	GND
10	GND	GPPL-1	-2V	-2V	Daisy chain 2- 2-in	Daisy chain 2- 2-out	GND
11	GND	GPPL-2	GPPL-3	GPPL-4	GPPL-5	GPP-6	GND
12	GND	Bus line2-0	+5V	+5V	Bunch Select 2 Bit 0	LVDS Turn clock Delay 2 +	GND
13	GND	Bus line2-1	+5V	+5V	Bunch Select 2 Bit 1	LVDS Turn clock Delay 2 -	GND
14	GND	Bus line2-2	+5VRET	+5VRET	Bunch Select 2 Bit 2	TTL Turn clock Delay 2 +	GND
15	GND	Bus line2-3	+5VRET	+5VRET	Bunch Select 2 Bit 3	TTL Turn clock Delay 2 -	GND
16	GND	Bus line2-4	+15V	+15V	Bunch Select 2 Bit 4	LVDS 40 MHz Clock 2 +	GND
17	GND	Bus line2-5	+15VRET	+15VRET	Bunch Select 2 Bit 5	LVDS 40 MHz Clock 2 -	GND
18	GND	Bus line2-6	-15VRET	-15VRET	Bunch Select 2 Bit 6	TTL 40 MHz Clock 2 +	GND
19	GND	Bus line2-7	-15V	-15V	Bunch Select 2 Bit 7	TTL 40 MHz Clock 2 -	GND

Table 6b: Pin allocations on J0 for slots 13 to 21 (Front view)

Pos	Row z	Row a	Row b	Row c	Row d	Row e	Row f
1	GND	HW Low Byte 1 bit 0	HW High Byte 1 bit 0		HW Low Byte 2 bit 0	HW High Byte 2 bit 0	GND
2	GND	HW Low Byte 1 bit 1	HW High Byte 1 bit 1		HW Low Byte 2 bit 1	HW High Byte 2 bit 1	GND
3	GND	HW Low Byte 1 bit 2	HW High Byte 1 bit 2		HW Low Byte 2 bit 2	HW High Byte 2 bit 2	GND
4	GND	HW Low Byte 1 bit 3	HW High Byte 1 bit 3		HW Low Byte 2 bit 3	HW High Byte 2 bit 3	GND
5	GND	HW Low Byte 1 bit 4	HW High Byte 1 bit 4		HW Low Byte 2 bit 4	HW High Byte 2 bit 4	GND
6	GND	HW Low Byte 1 bit 5	HW High Byte 1 bit 5		HW Low Byte 2 bit 5	HW High Byte 2 bit 5	GND
7	GND	HW Low Byte 1 bit 6	HW High Byte 1 bit 6		HW Low Byte 2 bit 6	HW High Byte 2 bit 6	GND
8	GND	HW Low Byte 1 bit 7	HW High Byte 1 bit 7		HW Low Byte 2 bit 7	HW High Byte 2 bit 7	GND
9	GND						GND
10	GND						GND
11	GND						GND
12	GND	Bunch Select 1 Bit 0	LVDS Turn clock Delay 1 +		Bunch Select 2 Bit 0	LVDS Turn clock Delay 2 +	GND
13	GND	Bunch Select 1 Bit 1	LVDS Turn clock Delay 1 -		Bunch Select 2 Bit 1	LVDS Turn clock Delay 2 -	GND
14	GND	Bunch Select 1 Bit 2	TTL Turn clock Delay 1 +		Bunch Select 2 Bit 2	TTL Turn clock Delay 2 +	GND
15	GND	Bunch Select 1 Bit 3	TTL Turn clock Delay 1 -		Bunch Select 2 Bit 3	TTL Turn clock Delay 2 -	GND
16	GND	Bunch Select 1 Bit 4	LVDS 40 MHz Clock 1 +		Bunch Select 2 Bit 4	LVDS 40 MHz Clock 2 +	GND
17	GND	Bunch Select 1 Bit 5	LVDS 40 MHz Clock 1 -		Bunch Select 2 Bit 5	LVDS 40 MHz Clock 2 -	GND
18	GND	Bunch Select 1 Bit 6	TTL 40 MHz Clock 1 +		Bunch Select 2 Bit 6	TTL 40 MHz Clock 2 +	GND
19	GND	Bunch Select 1 Bit 7	TTL 40 MHz Clock 1 -		Bunch Select 2 Bit 7	TTL 40 MHz Clock 2 -	GND

Table 7: Pin allocations on J0 for slots 12 (Front view)